CLAIMS

What is claimed is:

1. A method for forming multiple resistors on a substrate, comprising:

first providing a first resistor;

first depositing, patterning, and selectively etching a first dielectric layer over the first resistor;

second providing second resistor material over the first dielectric layer;

third providing landing pad material over the second resistor material; and

selectively etching said landing pad material and said second resistor material, where said selectively etching forms contacts for the first resistor in a first region, and forms a second resistor and associated contacts in a second region.

2. The method of claim 1, wherein said first providing includes providing chromium silicon (CrSi) material.

3. The method of claim 1, wherein said first providing includes providing nickel chromium (NiCr) material.

4. The method of claim 1, wherein said first providing includes providing a silicon substrate.

5. The method of claim 1, wherein said second providing includes providing nickel chromium (NiCr) material.

6. The method of claim 1, wherein said third providing said landing pad material includes providing titanium-nitride (TiN).

7. The method of claim 1, wherein said third providing said landing pad material includes providing titanium-tungsten (TiW).

8. The method of claim 1, wherein said first providing a first resistor includes providing a substrate.

9. The method of claim 8, wherein said first providing a first resistor includes depositing a second dielectric layer on top of the substrate.

10. The method of claim 9, wherein said first providing a first resistor includes depositing, patterning, and selectively etching a first resistor material on top of the second dielectric layer.

11. The method of claim 1, further comprising:

second depositing a second dielectric layer on said contacts for the first resistor, exposed portions of said second resistor, and exposed portions of said first dielectric layer.

12. The method of claim 11, further comprising:

appropriately repeating said first providing, said first depositing, said second providing, said third providing, said selectively etching, and said second depositing.

13. A method for forming a plurality of thin film resistors, comprising:

forming a first thin film resistor;

depositing and selectively etching a dielectric layer to provide contact openings for the first thin film resistor;

patterning and selectively etching landing pad material on a layer of second thin film resistor material in the contact openings to provide contacts to the first thin film resistor;

first selectively etching the landing pad material on the layer of the second thin film resistor material at an area away from the contact openings to form a second thin film resistor; and

second selectively etching the landing pad material above the second thin film resistor to expose the second thin film resistor, and to provide contacts for the second thin film resistor.

14. The method of claim 13, further comprising:

appropriately repeating said forming, said depositing, said patterning, said first selectively etching, and said second selectively etching, to form additional thin film resistors.

15. A method for forming a plurality of thin film resistors, comprising:

first providing a substrate;

first depositing a first dielectric layer on the substrate;

second depositing a first thin film resistor material on the first dielectric layer;

first patterning and selectively etching the thin film resistor material to form a first thin film resistor;

third depositing a second dielectric layer over the first thin film resistor and over the exposed portion of the first dielectric layer;

etching the second dielectric layer over portions of the first thin film resistor to provide contact openings for the first thin film resistor;

fourth depositing second thin film resistor material over portions of the first thin film resistor underlying the contact openings and over the second dielectric layer;

fifth depositing landing pad material over the second thin film resistor material;

second patterning and selectively etching the landing pad material and the second thin film resistor material over the contact openings to provide etch-stop contacts for the first thin film resistor;

third patterning and selectively etching the landing pad material and the second thin film resistor material at an area away from the first thin film resistor to form a second thin film resistor;

selectively etching the landing pad material on the second thin film resistor to expose the second thin film resistor, and to provide contacts to the second thin film resistor with remaining portions of the landing pad material;

sixth depositing a third dielectric layer over the etched landing pad material, exposed portion of the second thin film resistor, and exposed portion of the second dielectric layer; and

second providing shallow contacts to the first and second thin film resistor.

16. The method of claim 15, wherein said providing a substrate includes providing a silicon substrate.

17. An integrated circuit structure having thin film resistors, comprising:

a first dielectric layer;

a first thin film resistor disposed on said first dielectric layer over a first region;

a second dielectric layer disposed on said first dielectric layer and said first thin film resistor;

a plurality of contacts for the first thin film resistor having at least first and second layers, the first layer including second thin film resistor material, and the second layer including landing pad material, said plurality of contacts disposed on top edge portions of the first thin film resistor; and

a second thin film resistor having at least first and second layers, the first layer including said second thin film resistor material, and the second layer including said landing pad material, said second thin film resistor disposed on the second dielectric layer over a second region.

18. The method of claim 17, further comprising:

a third dielectric layer deposited on said plurality of contacts for the first thin film resistor, exposed portions of said second thin film resistor, and exposed portions of said second dielectric layer.

19. The method of claim 18, further comprising:

a plurality of metal contacts in the third dielectric layer, said metal contacts coupled to the first and second thin film resistors.

20. An integrated circuit including a plurality of thin film resistors, comprising:

a plurality of integrated structures, each structure successively disposed on top of a previous structure, each structure including:

a first dielectric layer;

a first thin film resistor disposed on said first dielectric layer over a first region;

a second dielectric layer disposed on said first dielectric layer and said first thin film resistor;

a plurality of contacts for the first thin film resistor having at least first and second layers, the first layer including second thin film resistor material, and the second layer including landing pad material, said plurality of contacts disposed on top edge portions of the first thin film resistor;

a second thin film resistor having at least first and second layers, the first layer including said second thin film resistor material, and the second layer including said landing pad material, said second thin

film resistor disposed on the second dielectric layer over a second region; and

a third dielectric layer deposited on said plurality of contacts for the first thin film resistor, exposed portions of said second thin film resistor, and exposed portions of said second dielectric layer.